pumps 40-1 to 40-n may be driven at a high power consumption stage.

Please **rewrite paragraph [37]** as follows:

Cond B8

[37] Accordingly, the charge pump device according to the present invention reduces power consumption by adjusting automatically the number of unit charge pumps in operation in accordance with the power consumption variation of an associated apparatus by detecting a level of a boosted voltage.

IN THE ABSTRACT:

Please **substitute the attached Abstract** for that originally filed.

IN THE CLAIMS:

Please **cancel claims 4, 6, 11, 13, 14, 16, and 17** without prejudice or disclaimer.

Please **rewrite claims 1, 2, 5, 8-10, 12, and 15** as follows:

Sub C1 B9

1. (Amended) A charge pump circuit for supplying a boosted voltage to a memory device, comprising:

a charge pump part constructed with first to nth unit charge pumps; and

a multi-level detector that detects a level variation of the boosted voltage and outputs a plurality of level detection signals for selectively driving the unit charge pumps, the multi-level detector including:

a voltage distributor for dividing the boosted voltage into first to nth voltage levels; and

first to nth level detectors for comparing the first to nth voltage levels with a reference level and generating the first to nth level detection signals.

Cont B9

2. (Amended) The charge pump device of claim **1**, further comprising:

an oscillator for producing a pulse signal in accordance with the first level detection signal from the first level detector; and

a logic operation part for logically operating the pulse signal of the oscillator and the second to nth level detection signal from the second to nth level detectors, and outputting the operated signal to the charge pump part.

B10 Sub C1

5. (Amended) The charge pump device of claim 1, wherein the second to nth unit charge pumps are selectively driven in

Cond B10

accordance with the level of the boosted voltage when the memory device is operated in an active state.

8. (Amended) The charge pump device of claim **1**, wherein the first voltage level is always lower than the reference level.

B11

9. (Amended) A charge pump device associated with a memory device, comprising:

Sub C1

a charge pump part including first to nth unit charge pumps to generate a boosted voltage;

a multi-level detector that detects a level of the boosted voltage and outputs first to nth level detection signals for selectively driving the unit charge pumps, wherein the first unit charge pump is always driven by the first level detection signal output from the multi-level detector, and each of the first to nth level detectors is composed of a different amplifier.

10. (Amended) The charge pump device of claim **9**, wherein the multi-level detector includes:

a voltage distributor for dividing the boosted voltage into first to nth voltage levels; and

first to nth level detectors for detecting a plurality of levels of the boosted voltage by comparing the first to nth

Cond B11

voltage levels divided by the voltage distributor with a reference level.

Sub B12

12. (Amended) The charge pump device of claim **10**, wherein the first voltage level is always lower than the reference level.

Sub C1 B13

15. (Amended) The charge pump device of claim **9**, wherein the second to nth unit charge pumps are selectively driven in accordance with the level of the boosted voltage when the memory device is operated in an active state.